

R16

Code No: 135BF

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech III Year I Semester Examinations, January/February - 2023

MICROPROCESSORS AND MICROCONTROLLERS

(Common to EEE, EIE)

Time: 3 Hours

Max. Marks: 75

Note: i) Question paper consists of Part A, Part B.

ii) Part A is compulsory, which carries 25 marks. In Part A, Answer all questions.

iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

- 1.a) List the dedicated interrupts of 8086 microprocessor. [2]
- b) Define macro with example. [3]
- c) What is the difference between microprocessor and microcontroller? [2]
- d) Explain PSW of 8051 microcontroller. [3]
- e) List out the important features of the A/D converter. [2]
- f) What is the significance of EA pin? [3]
- g) What is 'Thumb' in ARM processor? [2]
- h) Differentiate between CPSR and SPSR. [3]
- i) Write two features of Cortex processors. [2]
- j) Briefly explain about memory map of Cortex processors. [3]

PART – B

(50 Marks)

- 2.a) Explain the concept of segmented memory. What are the advantages? [5+5]
- b) Describe the implementation of pipelined process of 8086. [5+5]

OR

- 3.a) Write an assembly language program to count number of even and odd numbers in the array of sixteen bit numbers. [5+5]
- b) List out the shift and rotate instructions of 8086 microprocessor with examples. [5+5]

- 4.a) Explain the concept of memory organization of 8051 microcontroller. [5+5]
- b) Explain the addressing modes in 8051 microcontroller. [5+5]

OR

- 5.a) Draw the pin Diagram of 8051 microcontroller and explain the function of each pin in detail. [5+5]
- b) Write a program to count the numbers of 1's and 0's in 8-bit data stored. [5+5]

- 6.a) Draw the internal RAM organization of 8051 microcontroller and explain it. [5+5]
- b) Explain RS-232 Standards. [5+5]

OR

- 7.a) Explain the timer control register and timer mode control register. [5+5]
- b) Discuss about 8051 serial port programming. [5+5]

QA

QA

QA

QA

QA

QA

QA

QA

8.a) Draw the architectural block diagram of ARM and explain data flow referring each unit.

b) Explain the working of "Barrel shifter" with an example instruction and diagram. [5+5]

OR

9.a) Explain the three-stage pipelining implemented in ARM processor.

b) Explain the different exceptions in ARM processors. [5+5]

10.a) What are the advantages of Cortex processors.

b) Explain the architecture of Cortex processor. [5+5]

OR

11.a) What are the advantages of OMAP processors.

b) Explain the architecture of OMAP processor. [5+5]

QA

QA

QA

QA

QA

QA

QA

QA

---ooOoo---

QA

QA

QA

QA

QA

QA

QA

QA

QA

QA

QA

QA

QA

QA

QA

QA

QA

QA

QA

QA

QA

QA

QA

QA

QA

QA

QA

QA

QA

QA

QA

QA